南京拓品微电子有限公司

Datasheet

(TP7661A /B)

TP7661A/B DC-DC converter

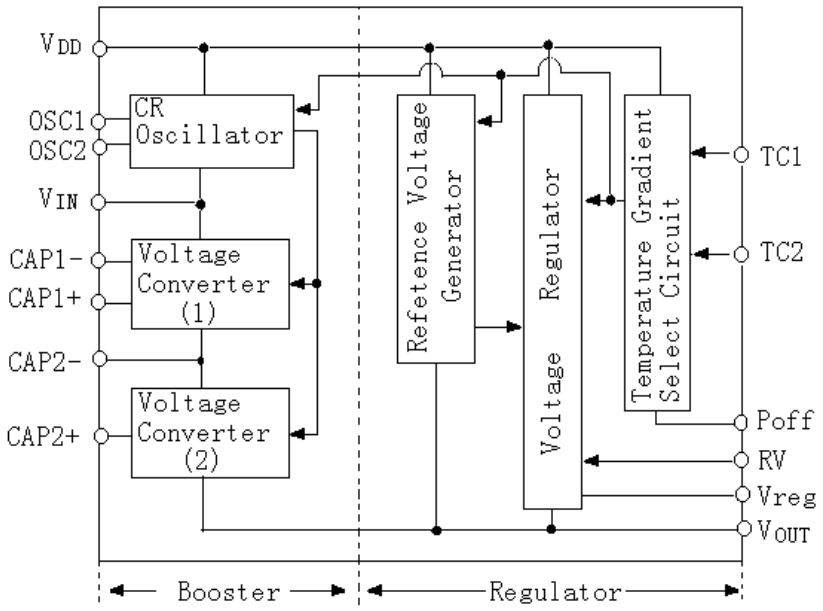
Product Introduction:

The TP7661A CMOS DC-DC converter is a low-power, easy-to-use power chip. Double voltage usage method: When the input negative voltage is -1.0~-8.0V, it can generate an output of -2.0~-16V; When the input positive voltage is 1.0~8.0V, it can generate an output of -1.0~-8.0V; Triple voltage usage: When the input negative voltage is -1.0~-6.0V, it can generate -3.0~-18.0V output, and when the input positive voltage is 1.0~6.0V, it can generate -2.0~-12.0V output. Three temperature gradient adjustment voltages are available for selection. PIN pin compatible with SCI7661. (TP7661B has the same performance as TP7661A except for the absence of Veleg and RV functions, and the PIN pin is compatible with SCI7661).

Product Features:

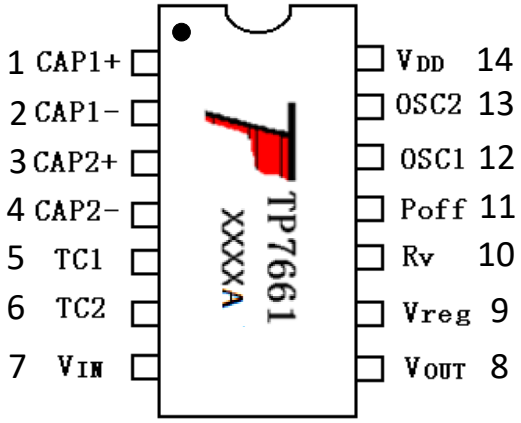
* High performance, low power consumption, ultra-low voltage startup
* Adopting soft breakdown technology to make product performance more stable and reliable
* Drive capability 50% higher than similar products
* Voltage conversion range: The maximum absolute input voltage at triple voltage is 1.0V~6.0V, and at double voltage is 1.0V~8.0V. The maximum voltage difference that the chip can withstand is 18.0V.
* Power conversion efficiency: typical value of 95%
* Can provide three temperature gradients for LCD: 0.1%/℃, 0.4%/℃, and 0.6%/℃
* The maximum current consumption when the chip power is turned off by an external signal is 2 μ A
* Two pieces in series VIN=-5V, VOUT=-20V
* Built in RC oscillator on chip
* Packaging form -------- SOP14

Working principle diagram



Package information:

SOP14:（TP7661B　pin9 and pin 10 have no function）



Pin　Function:

Pin Name	Pin Number	Function
CAP1+, CAP1-	1,2	double voltage connection capacitor terminal
CAP2+, CAP2-	3,4	Triple voltage connection capacitor terminal
TC1, TC2	5,6	Temperature gradient selection
VIN	7	Power input terminal (negative, VDD grounded)
VOUT	8	Triple voltage output terminal
Vreg	9	Adjust the voltage output terminal
Rv	10	Adjust the voltage control terminal
Poff	11	Vreg output on/off control terminal
OSC1,OSC2	12，13	External resistor terminal of oscillator
VDD	14	Power input terminal (grounded, VIN connected to the negative terminal of the power supply)

Recommended Operating Conditions:

parameter	symbol	MIN	MAX	UNIT	NOTE
starting voltage	VSTA		-1.0	V	Rosc = 1MΩ,
Double voltage termination voltage	VSTP	-1.0		V	Rosc = 1MΩ,
output-load current	IOUT		35	mA	
Oscillator frequency	fosc	10	1000	KHz	
External resistor of oscillator	Rosc	0	2000	KΩ	
capacitance	C1，C2，C3	0．33		μF	
Adjustable resistor	RRV	100	1000	KΩ	

Extreme working conditions:

parameter	symbol	MIN	MAX	UNIT	NOTE
Input power supply voltage	VI	-18.0/3	0.5	V	Triple voltage
		-8.5	0.5	V	double voltage
Input voltage	VI	VIN-0.5	0.5	V	OSC1, Poff
		VOUT-0.5	0.5	V	TC1, TC2, Rv
Output voltage	Vo	-18.0		V	
Allow power consumption	Pd		500	mW	
operation temperature	Topr	-30	85	℃	Plastic sealing
storage temperature	Tstg	-55	150	℃	
Welding temperature and time	Tsol	260℃ ,10s			

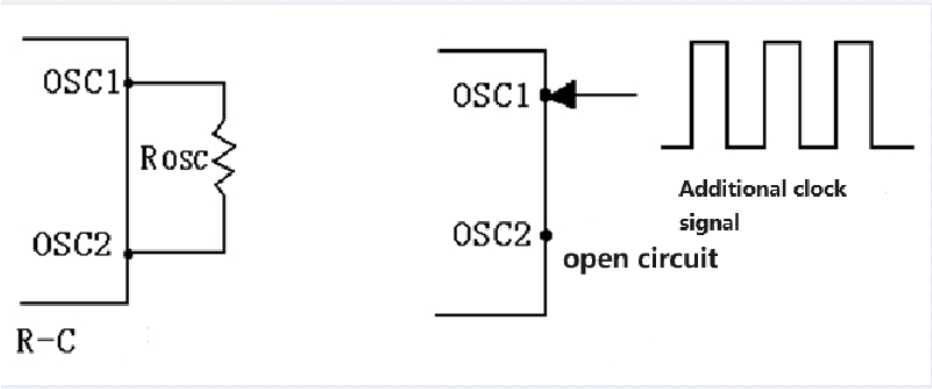
Electrical Characteristics (VDD=0V,VIN=-5V,Ta=-30~85℃)

parameter	symbol	Test conditions	MIN	TYP	MAX	unit
Input power supply voltage	Vi	Negative voltage input	-6.0		-1.0	V
Output voltage	Vo	Negative voltage input	-18.0		-3.0	V
	Vreg	RL= ∞,RRV=1MΩ,Vo=-18V	-18.0		-2.6	V
Voltage doubling no-load current	Iopr1	RL= ∞， Rosc=1MΩ		60	100	μA
Adjusting the current	Iopr2	RL= ∞，RRV=1MΩ，Vo=-15V		5.0	12.0	μA
quiescent current	IQ	TC2=TC1=VOUT, RL=∞			2.0	μA
Oscillator frequency	fosc	Rosc = 1MΩ	20	30	40	KHz
Voltage doubling power conversion efficiency	Peff	IOUT=5mA	90	95		%
Output internal resistance	ROUT	IOUT=10mA		100	140	Ω
Adjust output voltage fluctuations	ΔVreg/ (ΔVOUT• Vreg)	-18V<VOUT<-8V,Vreg=-8V, RL= ∞, ,Ta=25℃		0.2		%/V
Adjust output load fluctuations	$\frac{\Delta Vreg}{\Delta IOUT}$	Vo=-15V， Vreg=-8V, 0<IOUT<10 mA,, Ta=25℃ TC1=VDD, TC2=VO		5		Ω
Adjust the output saturation resistance	RSAT	RSAT=(Vreg–VOUT)/IOUT, 0<IOUT<10mA, RV=VDD Ta=25℃		8		Ω
Adjusting voltage	VRV0	TC2=VOUT,TC1=VDD,Ta=25℃	-2.3	-1.5	-1.0	V
	VRV1	TC2= TC1=VOUT,Ta=25℃	-1.7	-1.2	-0.9	V
	VRV2	TC2=VDD,TC1=VOUT,Ta=25℃	-1.1	-0.9	-0.8	V
temperature gradient	CT0	$CT=\frac{\lvert Vreg(50℃)\rvert - \lvert Vreg(0℃)\rvert}{50℃-0℃} \times 1/\lvert Vreg(50℃)\rvert \times 100$	-0.25	-0.1	-0.06	%/℃
	CT1		-0.5	-0.4	-0.2	%/℃
	CT2		-0.7	-0.6	-0.5	%/℃
Input leakage current	IL	Poff,TC1,TC2,OSC1,RV			2.0	μA

Circuit Description

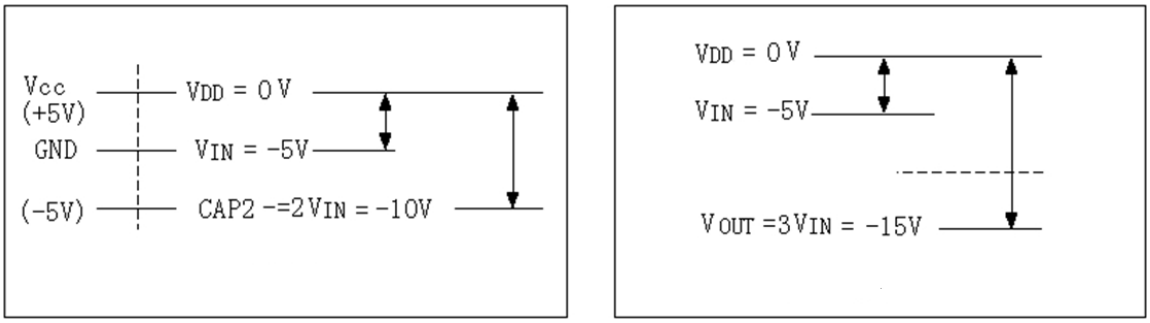
1.R-C oscillating

This chip has a built-in RC oscillator and can also be connected to external oscillation signals。

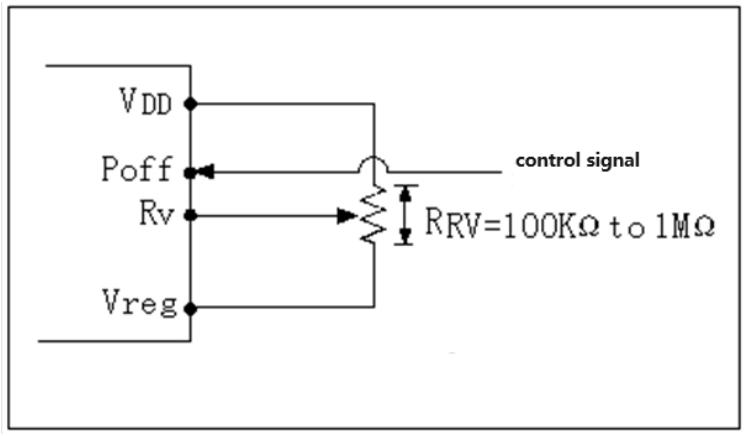


2. Voltage reversal

By oscillating the signal, a reverse voltage of 2/3 times the input voltage (VIN) can be obtained.



3. Reference voltage generation and voltage adjustment



4. Temperature gradient selection

This chip can provide a voltage with a suitable temperature gradient to drive liquid crystal (LCD) (this voltage is applied between VDD and Vreg)

Poff	TC2	TC1	temperature gradient	Vreg output	oscillator	NOTE
1（VDD）	L(VOUT)	L(VOUT)	-0.4%/℃	ON	ON	
1	L	H(VDD)	-0.1%/℃	ON	ON	
1	H(VDD)	L	-0.6%/℃	ON	ON	
1	H	H	-0.6%/℃	ON	OFF	cascade
0 (VIN)	L	L		OFF（High resistance)	OFF	
0	L	H		OFF（High resistance）	OFF	
0	H	L		OFF（High resistance）	OFF	
0	H	H		OFF（High resistance）	ON	No adjustment function

Note: Poff has different low levels from TC1 and TC2

Typical Circuit:

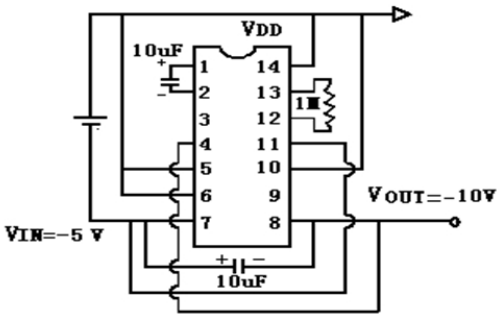


Figure 1.Negative voltage twice output

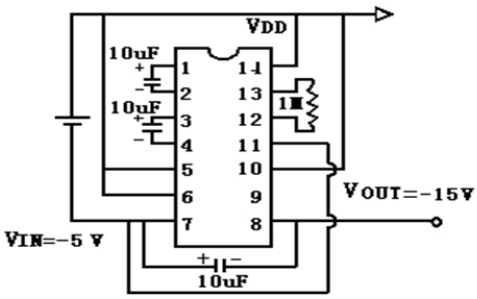


Figure2.Negative voltage triple output

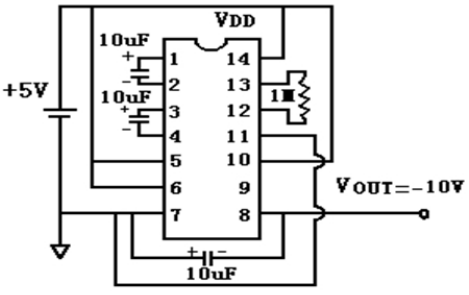


Figure3.Positive voltage triple output

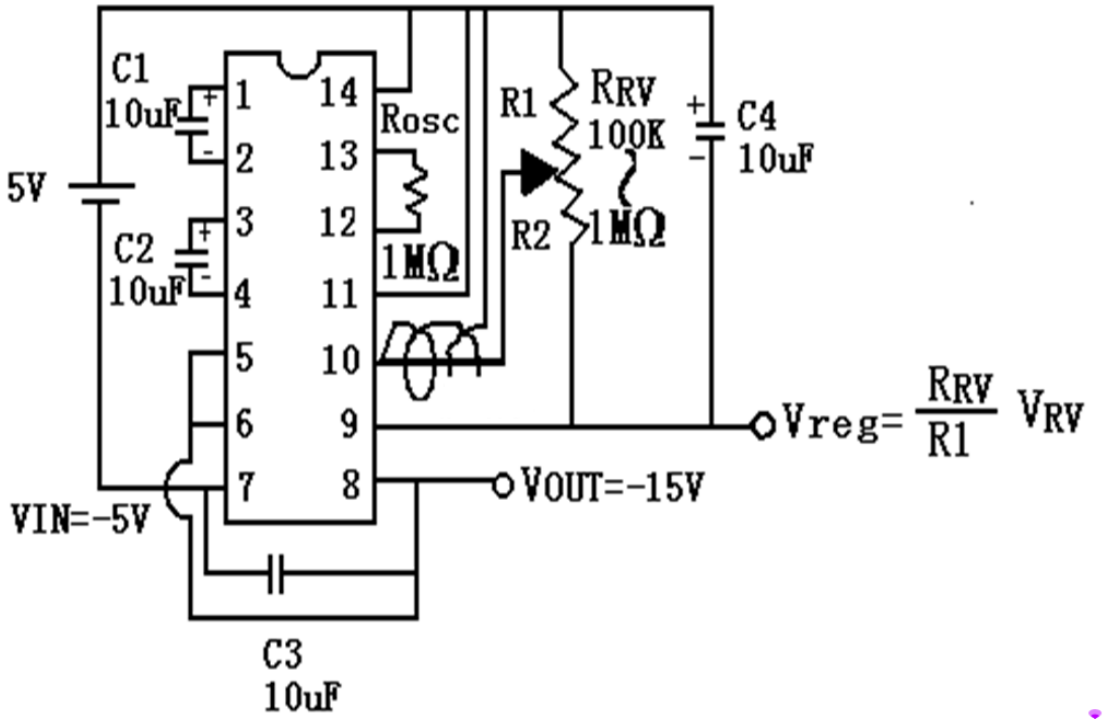


Figure 4: Negative voltage input, triple voltage output, and VOUT and Vreg can be output simultaneously. Adjusting R1 and R2 can make the Vreg output different, and Vreg also has temperature gradient function

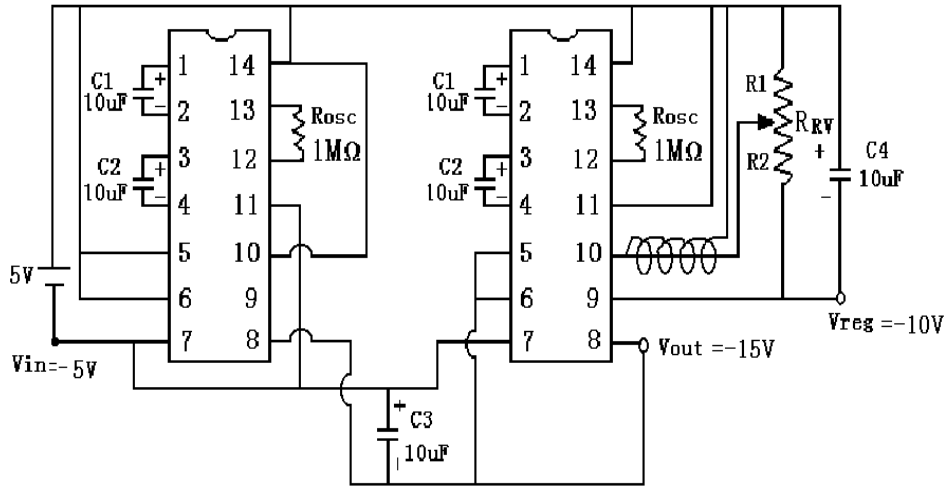


Figure 5: Parallel connection of n chips can reduce the output impedance ROUT to approximately 1/n.

All parallel chips only need to share one filtering capacitor C3, and all parallel chips can only have one chip with adjustable voltage output

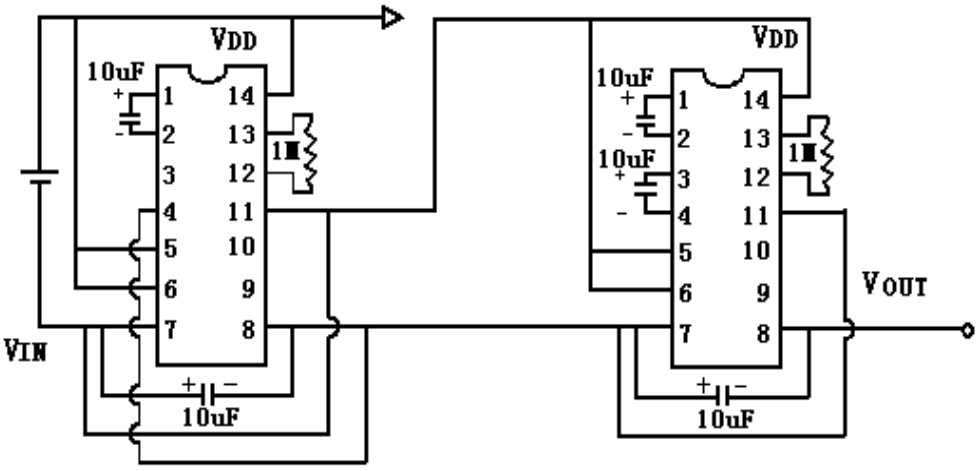
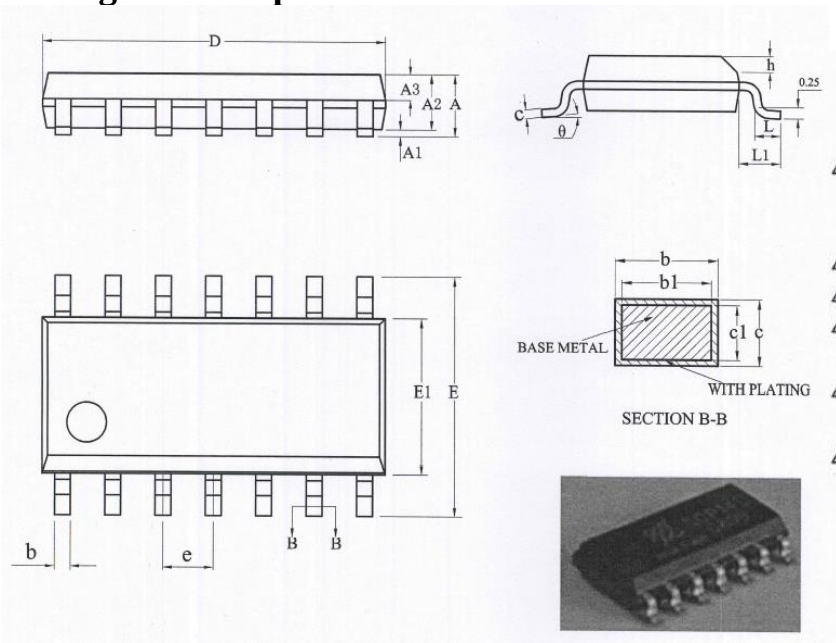


Figure 6: Connecting two chips in series can result in an output voltage of approximately VOUT=4VIN.
Please note that VDD-VIN should be less than 6.0V

Package Description



	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
	A	—	—	1.75
2	A1	0.10	—	0.225
	A2	1.30	1.40	1.50
	A3	0.60	0.65	0.70
1	b	0.39	—	0.47
1	b1	0.38	0.41	0.44
1	c	0.20	—	0.24
	c1	0.19	0.20	0.21
1	D	8.55	8.65	8.75
	E	5.80	6.00	6.20
1	E1	3.80	3.90	4.00
	e	1.27BSC		
	h	0.25	—	0.50
	L	0.50	—	0.80
	L1	1.05REF		
	θ	0	—	8°